

**In the Claims:**

1. (canceled)
2. (currently amended) An on-chip capacitor, comprising:  
first and second metal patterns each in first and second levels;  
wherein said first pattern of said first level is connected to said first pattern of said  
second level by conducting vias;  
wherein said second pattern of said first level is connected to said second pattern of  
said second level by conducting vias; and  
wherein said first pattern and said second pattern form contacts for a capacitor;  
~~The capacitor of Claim 1,~~ wherein said first and second levels are separated by a material of first dielectric constant, and said first and second patterns are separated by a material of a second dielectric constant, and wherein said first dielectric constant is greater than said second dielectric constant.
3. (canceled)
4. (currently amended) The capacitor of Claim 2 +, wherein vias extend from said first and said second metal patterns and do not connect to metal patterns of any other level.  
5-6 (canceled).

7. (currently amended) An integrated circuit structure, comprising:  
a first layer having a first metallization pattern comprising at least two metal lines;  
a second layer having a second metallization pattern comprising at least two metal  
lines;  
wherein said first and second metallization patterns are connected by conducting  
vias to form a capacitance;

~~The integrated circuit of Claim 5,~~ wherein said vias extend at least half the length of  
said first and said second metallization patterns where they face each other.

8 (canceled).

9. (currently amended) An method of fabricating an on-chip capacitor, comprising  
the steps of:

providing a first stack of metal lines, each line of said first stack of lines separated  
from an adjacent line of said first stack by a second dielectric;

providing a second stack of metal lines, each line of said second stack of lines  
separated from an adjacent line of said second stack by said second dielectric and laterally  
separated from said first stack by a first dielectric material having a higher dielectric  
constant than said first dielectric;

providing first conducting vias connecting wherein two or more of said metal lines  
of said first stack ~~are vertically connected by~~ the first conducting vias; and

providing second conducting vias vertically connecting wherein two or more of said  
metal lines of said second stack ~~are vertically connected by~~ the second conducting vias; and  
wherein said first stack and said second stack ~~provide~~ providing two terminals of a  
capacitor.

10. (previously presented) The method of Claim 9, wherein said vias are laterally  
separated by a second dielectric material, and said dielectric constant of said second  
dielectric material is greater than the dielectric constant of said first dielectric material.

11. (previously presented) The method of Claim 9, wherein said vias extend over  
half the length of said metal lines to which they connect.

12. (currently amended) An method of fabricating an on-chip capacitor, comprising  
the steps of:

providing first and second interdigitated metal patterns having a first dielectric  
therebetween and providing lateral capacitance therebetween;

providing elongated vias having a second dielectric therebetween and which  
provide lateral capacitance therebetween, and which are parallel and electrically  
connected to each of said first and second patterns, said first dielectric having a higher  
dielectric constant than said second dielectric;

wherein said first and second metal patterns, in combination with said elongated  
vias, define defining a capacitor.

13. The method of Claim 12, wherein said elongated vias extend over more than  
half the peripheral length where said first and said second interdigitated metal patterns  
face each other.

14. The method of Claim 12, wherein said elongated vias also provide vertical  
connection from said respective metal patterns to corresponding metal patterns in one or  
more other layers of metallization.

15. The method of Claim 12, wherein said elongated vias provide more lateral  
capacitance than said interdigitated metal patterns do.

16. The method of Claim 12, further comprising vias attached to said first and  
second patterns that do not connect to any other metal patterns.